IN THE SPECIFICATION

Please amend the specification as shown below.

Please replace the paragraph beginning on page 1, line 7 with the following:

The present invention relates to a method for forming contact openings ~~towards~~ to selected locations of the surface of a MOS integrated circuit.

Please replace the paragraphs beginning on page 1, line 11 with the following:

For MOS integrated circuits in which the primary structures are of very small dimensions, for example, in which the gate structures have a length smaller than one tenth of a micrometer, one of the limitations to miniaturization is the forming of contact openings ~~towards~~ to semiconductor areas of the structure. This will be illustrated in relation with Fig. 1.

The left-hand portion of Fig. 1 illustrates an example of a MOS transistor formed in an active area of a substrate 1 delimited by shallow trenches 2 filled with an insulator (STI). This MOS transistor comprises an insulated gate 3 formed on a thin gate insulator layer 4. Gate 3 is ~~currently~~ conventionally made of polysilicon and gate insulator 4 is silicon oxide, although there currently is a tendency to preferring other insulators with a smaller dielectric constant. This gate is used to delimit a first implanted area 5 in the active area of substrate 1. Then, the gate is surrounded with spacers, for example, as shown, with silicon nitride spacers 7 having an L-shaped cross-section and separated from the gate and from the substrate by a very thin oxide layer. The spacers are used to delimit more heavily-doped source and drain regions 8 and 9 in substrate 1. Preferably, the upper surface of gate 3 and the upper surfaces of source and drain regions 8 and 9 are formed of a layer of a metal silicide to improve the conduction and favor the contact making. Metal silicide areas are indicated in Fig. 1 and in the following drawings by a thick line with no reference numeral.

In the right-hand portion of Fig. 1, two transistors ~~analog~~ analogous to that of the left-hand portion, arranged side by side without being separated by an insulating area, have been

shown. The two adjacent transistors have a common drain/source region 11 on which a contact may be desired to be formed.

Please replace the paragraph beginning on page 2, line 6 with the following:

A conventional method for forming a contact opening is illustrated in Fig. 2. The entire structure illustrated in Fig. 1 is covered with a protective layer 20, for example, a silicon nitride layer. An insulating layer 21, re-etched by chem-mech etch to have a planar upper surface, is then deposited. Layer 21 is covered with a mask 22. It should be noted that this insulating layer remains in place at the end of the process and must be of fine quality. It results, for example, ~~of~~ from a high-density plasma deposition.

Please replace the paragraphs beginning on page 2, line 20 with the following:

The opening of the first contact ~~towards~~ to drain/source region 8 poses no critical problem since it is possible to overflow with no inconvenience above insulating layer 2.

However, the opening of the second contact ~~towards~~ to drain/source region 11 ~~intermediary~~ intermediate between two adjacent transistors poses critical problems given the involved dimensions. Indeed, the accuracy of the positioning of mask 22 with respect to the previously-formed layers is on the order of 80 nm. This difference is smaller, in the context of the above-described example, than the distance between region 11 and the tops of the adjacent gates 3. Thus, in case of an excessive shifting of opening 24 of the mask, the silicon nitride above region 11 and above one of the adjacent gates 3 will have to be etched at the same time, which results in a risk of short-circuit after metallization. This compels to ~~increase~~ increasing the transistor dimensions ~~only~~ in order to solve this problem of contact opening forming accuracy.

Please replace the paragraph beginning on page 3, line 12 with the following:

To achieve ~~this object~~ these and other objects, the present invention provides a method for forming contact openings in various locations of the upper surface of an integrated circuit comprising raised areas, some openings called critical openings having to be formed between two neighboring raised areas, comprising the steps of:

Please replace the paragraph beginning on page 4, line 1 with the following:

According to an embodiment of the present invention, the oblique ~~implantation~~ irradiation is performed under an angle from 45 to 60°.

Please replace the paragraph beginning on page 4, line 32 with the following:

More specifically, Fig. 3 shows the structure according to the present invention at the same stage as described in relation with Fig. 2, that is, after deposition of a protection layer 20, of a planarized insulating layer 21, and of a masking layer 22. However, as will be noted hereafter, layer 21 is then removed in the method according to the present invention and ~~must~~ should not necessarily exhibit excellent dielectric qualities. Layer 21 may thus for instance be a simple resin layer, which simplifies the manufacturing.

Please replace the paragraph beginning on page 7, line 112 with the following:

- the structure is coated with a second protection layer which, in the specific described embodiment, is a polysilicon layer but which may generally be made of any material ~~likely to have~~ that has etch properties which vary according to whether it has been irradiated or not, and